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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,691	04/08/2004	Robert A. Abraham	10031136-1	8538

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EXAMINER	
GOODLEY, JAMES E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/820,691	ABRAHAM ET AL.
	Examiner	Art Unit
	James E. Goodley	2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 8 is objected to because of the following informalities: there is no antecedent basis for "the voltage shift-down mechanism". It appears that claim 8 should depend from claim 4 instead of claim 2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 15-17 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Lo et al. (US 6,046,646)***, hereinafter Lo (of record).

Regarding **claims 1-5, and 15-17**, lines 8-15 of column 3, lines 1-11 of column 6, and Fig. 6 of Lo show a method for reducing EMI in a spread spectrum clock generation PLL circuit (as mentioned in the abstract) comprising: a voltage controlled oscillator (VCO) [324] that includes an input [317] coupled to a voltage control node [input to VCO] and an output [326] for generating a spread spectrum clock signal [F_{VCO}] with a frequency which is proportional to the input control voltage and a VCO input voltage modulation mechanism [330'] coupled to the input voltage control node for modulating the voltage at the control node by including in the voltage modulation mechanism: a

voltage shift-up mechanism [334'] for pulling up the voltage at the VCO input node by injecting current into that node, wherein the modulation mechanism generates a shift-up control signal [triangular input directly to left of switch to engage 334'] to input to the shift-up mechanism and a shift-up control enable signal [346] to input to the shift-up mechanism; and similarly, a voltage shift-down mechanism [336'] for pulling down the voltage at the VCO input node by drawing current from that node, wherein the modulation mechanism generates a shift-down control signal [triangular input directly to left of switch to engage 336'] to input to the shift-down mechanism and a shift-down control enable signal [348] to input to the shift-down mechanism.

Regarding **claims 19-20**, Fig. 6 of Lo shows the method of claim 15 and the circuit of claim 1 respectively, further comprising a P-counter [feedback divider 'divide by N' 328] that includes an input coupled to the VCO [324], a register for storing a single P value [single flip-flop inherently in device 328] and an output [310]; a Q-counter [reference divider 'divide by M' 304] that includes an input [302] for receiving a reference frequency [F_{ref}] and an output [306]; a phase detector [308] that includes a first input [306] coupled to the output of the Q counter and a second input [310] coupled to the output of the P counter and an output ["UP"] for generating a control signal [317]; a charge pump [312] coupled to the phase detector for receiving the control signal and selectively charging and discharging the voltage control node based on the control signal; and a loop filter [318].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo (of record) in view of ***Ma (US 2002/0075050 A1)***.

Regarding **claims 6-7**, Lo shows the circuit of claim 2 showing a voltage shift-up current source but does not specifically show, "wherein the voltage shift-up mechanism includes a first transistor having a drain electrode coupled to a first predetermined voltage, a source electrode, and a gate electrode for receiving a first shift-up control signal; a second transistor having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to the VCO input voltage node, and a gate electrode for receiving a shift-up control enable signal; a plurality of transistors coupled in parallel to the first transistor; wherein each transistor includes a drain electrode that is coupled to the first predetermined voltage, a source electrode that is coupled to the drain electrode of the second transistor, and a gate electrode for receiving a corresponding shift-up control signal".

However, paragraphs 54 and 55 and Figs. 2, 3 and 8 (with reference numerals of Fig. 8) of Ma show a charge-pump circuit for use in a duty-cycle regulator including a voltage shift-up mechanism [PUMP 1] including a first transistor [PMOS transistor having signal 'EN_SNK_0-' applied to its base] having a drain electrode coupled to a

first predetermined voltage [V_{DD}], a source electrode and a gate electrode for receiving a first shift-up control signal [EN_SNK_0-];

a second transistor [any of the 3 PMOS transistors directly adjacent 'PUMP 1' and applied to the gate an external current reference] having a drain electrode coupled to the source electrode of the first transistor, a gate electrode for receiving a shift-up control enable signal [external signal applied to the gate of second transistor]; a plurality of transistors [other two transistors shown with the same external signal applied to their gates] coupled in parallel to the first transistor wherein each transistor includes a drain electrode that is coupled to the first predetermined voltage, a source electrode that is coupled to the drain electrode of the second transistor, and a gate electrode for receiving a corresponding shift-up control signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the voltage shift-up mechanism in the circuit of Lo by including the weighted current-sourcing arrangement noted in Ma for the purpose of having finer control for raising the voltage at the input of the VCO of Lo in the oscillator loop, thereby more finely tuning the oscillation frequency.

Regarding **claims 8-9**, Lo shows the circuit of claim 4, showing a voltage shift-down current source but does not specifically show, "wherein the voltage shift-down mechanism includes a first transistor having a drain electrode coupled to the VCO input voltage node, a source electrode, and a gate electrode for receiving a shift-down control enable signal; a second transistor having a drain electrode coupled to the source electrode of the first transistor, a source electrode coupled to a second predetermined

voltage, and a gate electrode for receiving a shift-down control signal; a plurality of transistors coupled in parallel to the second transistor; wherein each transistor includes a drain electrode that is coupled to the source of the first transistor, a source electrode that is coupled to the second predetermined voltage, and a gate electrode for receiving a corresponding shift-down control signal".

However, paragraphs 54 and 55 and Figs. 2, 3 and 8 (with reference numerals of Fig. 8) of Ma show a charge-pump circuit for use in a duty-cycle regulator including a voltage shift-up mechanism [PUMP 2] including a first transistor [NMOS transistor having signal 'EN_SRC_0' applied to its base] having a drain electrode coupled to a first predetermined voltage [ground], a source electrode and a gate electrode for receiving a first shift-down control signal [EN_SRC_0];

a second transistor [any of the 3 NMOS transistors directly adjacent 'PUMP 2' and applied to the gate an external current reference] having a drain electrode coupled to the source electrode of the first transistor, a gate electrode for receiving a shift-down control enable signal [external signal applied to the gate of second transistor]; a plurality of transistors [other two transistors shown with the same external signal applied to their gates] coupled in parallel to the first transistor wherein each transistor includes a drain electrode that is coupled to the first predetermined voltage, a source electrode that is coupled to the drain electrode of the second transistor, and a gate electrode for receiving a corresponding shift-down control signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the voltage shift-down mechanism in the circuit of Lo by

including the weighted current-sourcing arrangement noted in Ma for the purpose of having finer control for lowering the voltage at the input of the VCO of Lo in the oscillator loop, thereby more finely tuning the oscillation frequency.

Regarding **claims 11-12, 14 and 21**, the device of Lo in view of Ma shows the circuit of claims 1 and 5 respectively, wherein the phase locked loop (PLL) modulation control circuit includes a plurality of programmable delay cells (PDCs) [transistors with their gates fed with signals 'EN_SNK_0-' – 'EN_SNK_2-' and 'EN_SRC_0' – 'EN_SRC_2'] for generating the shift-up control signals and the shift-down control signals; wherein the time delay (Delta(t)) of the delay cells is based on the modulation frequency and the number of modulation bits; wherein the delay cells are implemented as one of software and hardware."

Regarding **claim 13**, Lo in view of Ma discloses the circuit of claim 12, but does not specifically mention "wherein the time delay of the delay cells are also determined by stability considerations for the PLL and the VCO characterization." However, it is inherent that the time delay constants of any components put into a phase locked feedback loop will always need to be subject to stability considerations in the loop as a whole in order for the loop to function as an oscillator.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of ***Chang (US 6,606,005)*** (both of record).

Regarding **claim 10**, Lo shows the circuit of claim 1 except being, "integrated in one of personal computers (PCs), computing devices, computer peripherals, office

equipment, printers, network equipment, and other electronic applications where EMI reduction is needed".

However, lines 13-23 in column 1 of Chang teach spreading the spectrum of a clock generator on the motherboard of a computer in order to reduce EMI.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the spread spectrum clock generator as taught by Lo on a computer motherboard in order to reduce noise generated by a traditional clock as taught by Chang.

Response to Arguments

Applicant's arguments regarding claims 1-5, 15-17 and 19-20 filed 11/11/2005 have been fully considered but they are not persuasive. It is inherent that for the modulation mechanism 330' in Fig. 6 of Lo to function, it must provide control signals to charge pump 332' to provide current to charge capacitor 320 in loop filter 318. Clearly, the modulation voltage at node 344 is coupled to VCO input node 317 through resistor 319 and will likewise provide a modulation voltage at node 317 via the voltage drop across resistor 319.

Applicant's arguments regarding the elements in Chang and Tiede, with respect to the rejection(s) of claim(s) 6-9 and 11-14 under 35 USC § 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of ***Ma (US 2002/0075050 A1)***.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (combination of references under 35 USC § 103 to reject claims 6-9 and 11-14), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Although the detailed charge pump arrangement claimed in claims 6-9 and 11-14 are not expressly disclosed in Lo, a generic charge pump circuit is shown. It is noted that any charge pump may be used that performs the voltage shift-up and shift-down functions as claimed. Thus, there is suggestion to combine the reference of Ma with the reference of Lo.

It is acknowledged and appreciated that informalities have been corrected in claim 11 however, objection to claim 8 still stands, as claim 8 depends on claim 2, but refers to the voltage shift-down mechanism, rather than the voltage shift-up mechanism.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Non-Patent literature document **"Charge-Pump Phase-Lock Loops"** by Floyd M. Gardner – IEEE Transactions on Communication, Vol. Com-28, No.11 November 1980.

Fax/Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James E. Goodley. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JG

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